

MINISTRY OF EDUCATION AND SCIENCE OF UKRAINE
ZAPORIZHZHA NATIONAL TECHNICAL UNIVERSITY

Methodical Instructions

to laboratory works on discipline
"The basics of electronics and microcircuitry" part 2
for students of specialty
141 -"Electrical power engineering, electrical engineering and
electromechanics" of all forms of education

2019

Methodical Instructions to laboratory works on discipline "The basics of electronics and microcircuitry" part 2 for students of specialty 141 - "Electrical power engineering, electrical engineering and electromechanics" of all forms of education /Comp.: M.O.Polyakov, L.S. Skrupskaya. – Zaporizhzhya: ZNTU, 2019. – 23 p.

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CONTENT

Introduction.....	4
Laboratory work 1.....	5
Laboratory work 2.....	9
Laboratory work 3.....	14
Laboratory work 4.....	17
Laboratory work 5.....	20
Recommended literatur.....	24

INTRODUCTION

The purpose of the laboratory work is to consolidate the theoretical material from the discipline "Fundamentals of Electronics and Microcircuits" into Part 2 of the "Devices" in practice. For the study of electronic devices, the Electronics Workbench (EWB) schematic design model package is used - the development of the company Interactive Image Technologies. The advantage of computer simulation is the large variety of electronic elements and measurement tools to create an electronic circuit, the impossibility of its damage and a high level of electrical safety.

The methodical instructions contain a description of 5 laboratory works on the topics of the study of combinational knots, triggers, meters, voltage stabilizers, DACs and ADCs, power regulators.

Student is obligated to study theoretical material, to perform practical tasks and to make a report on laboratory work, which will have the main sections:

- name of laboratory work;
- its purpose;
- schemes of experiments, tables, graphs, calculations, conclusions.

The report must be made in accordance with STA 1596 and protected.

LABORATORY WORK 1

Objective: the structure and operating principle of combination units.

Brief theoretical data: A logical node is a device that processes information digitally. Logical nodes are subdivided into combinational and memory nodes. The main property of combinational nodes - the input vector X uniquely determines the output Y . The main difference between the combinational nodes and the memory nodes is that the outputs in the memory nodes depend on the state (the previous work cycle). Typical logical nodes: decoder, multiplexer, binary adder, code converter.

Decoder is a logical device that converts the binary code of the number entered to the input into a signal on one of its outputs. The decoder is designed to convert the code information records into counters and registers into control signals and to transmit them to the control system's operating elements in the display device. The decoder scheme (Fig.1.1) has several inputs and outputs. On the inputs A, B, C of the decoder comes the binary code of the number. For each code number the signal corresponds to one of 8 decoder outputs.

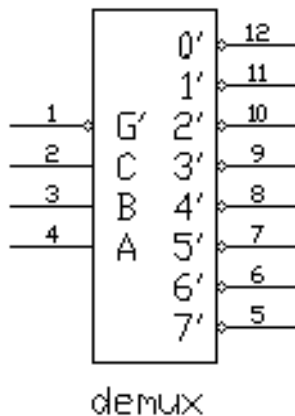


Figure 1.1 – Decoder

Inputs: G', A, B, C . Outputs: $0' - 7'$.

Motion of work

Experiment №1. – Reception of the decoder truth table

1 Build the decoder schema shown in Figure 1.2 (file 13_01 in the examples).

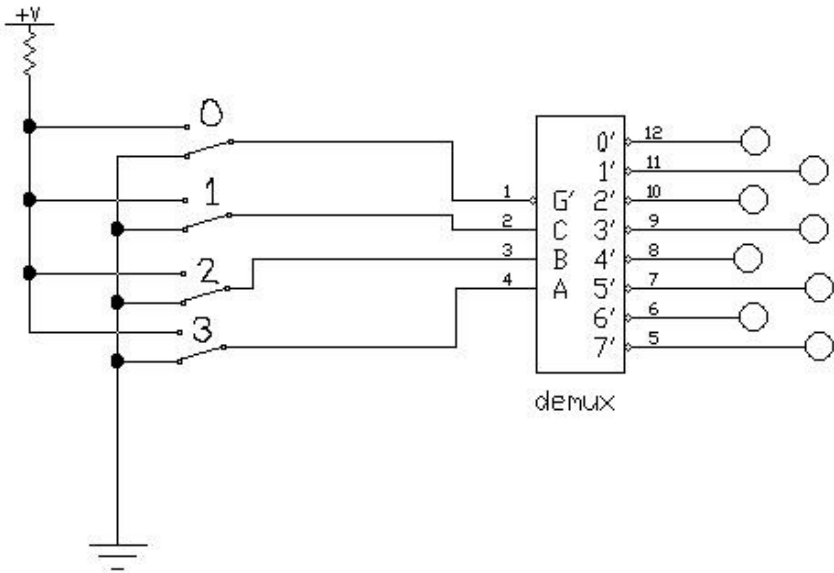


Figure 1.2 - Diagram of connecting the decoder "3 to 8"

2. Fill the table of truth of the device (Table 1.1) - only 16 states, observing the outputs of the decoder in various combinations of its inputs. Operations are performed by changing the states using the 0 to 3 switches.

Table 1.1 - Dependence of decoder outputs from inputs

G'	C	B	A	0	1	2	3	4	5	6	7
0	0	0	0								
...								
1	1	1	1								

Experiment number 2 - Realization of arbitrary logic function by means of a decoder

1 Draw the schema shown in Figure 1.3, which implements the function $A'B'C' + AB + BC$ (you can modify file 13_03 in the examples)

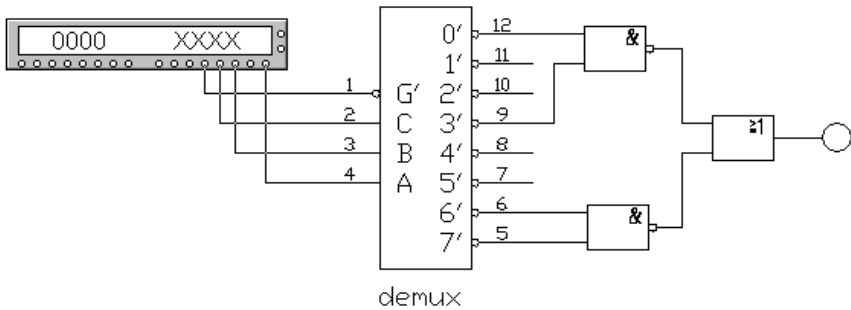


Figure 1.3- Realization of a given logic function using a decoder

2 Program the word generator as shown in Fig. 1.4

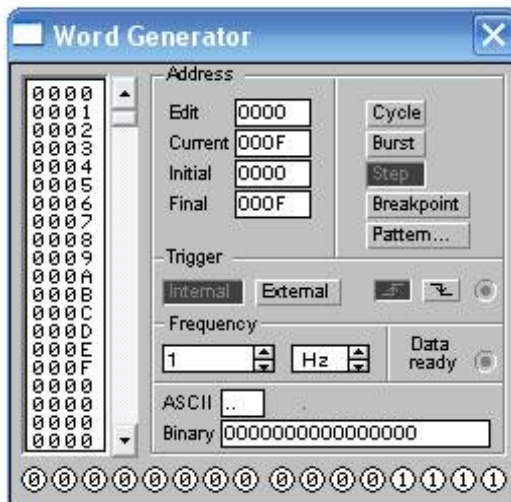


Figure 1.4 - Programming the word generator

3 Fill in the table 1.2 for all combinations of input values, to do this, run the schema to run and press the "step" button in the word generator, to fix the states at the output of the circuit.

4 Using the "Logic converter" specify the truth of the table in paragraph 5 as shown in Fig. 1.5

Table 1.2 - Truth Table for all combinations of input quantities

G'	C	B	A	Output
0	0	0	0	
...	
1	1	1	1	

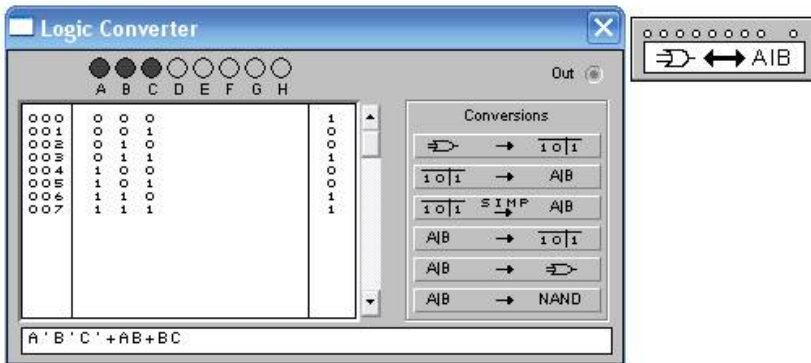


Figure 1.5- Specifying the truth table in the "Logic converter"

5. Convert the truth table to the formula implemented by the decoder (button 101 simp $\rightarrow A | B$). Compare the result with the original formula

Experiment number 3 - Realization of arbitrary logic function

1. Develop a scheme that implements the logical function proposed by the instructor
2. Test the developed scheme according to the method described in experiment number 2.

Control questions

- 1 Determination of the combinational node, its difference from the node with memory.
- 2 Varieties of combinational knots.
- 3 Principle of operation of the decoder and multiplexer.
- 4 Realization of arbitrary logic function by means of decoder.
- 5 Areas of use decoder, multiplexer.

LABORATORY WORK 2

Objective: to study the structure and principle of operation of RS, JK - triggers, counters; learn to design counters with a given conversion factor.

Brief theoretical data: in order to turn the combinational node into a memory node, use feedback. The memory node is characterized by two characteristic equations:

a) the outputs function $Y = f(X, S)$

де Y – output signal; X - input signal; S – state.

б) the transition function

$$S^{t+1} = f(S^t, X),$$

where S^t - state at the current time, S^{t+1} – state at the next time.

Typical nodes with memory: trigger, counter, and register.

A trigger is an elementary memory node that can be in one of the two states of "0" or "1", and has two outputs of straight and inverse. By the functions, the triggers are divided into: RS - triggers, D - triggers, T - triggers, JK triggers and others.

RS-trigger has two installation inputs: S (set-set) and R (reset-reset) settings, which are fed by incoming signals from external sources. When applying to the input of the installation of the active level of the logical signal, the trigger is set to "1", and when the active level of the logical signal is applied to the input, the reset trigger is set to "0". If at both inputs of the trigger passive logic levels of the input signal, then the trigger will save the previous state of the outputs. Each of these states is stable and is supported by feedback actions.

The JK-type trigger has a more complex, compared to the RS-trigger, internal structure, and wider functionality. In addition to the J and K information inputs, and the direct and inverse outputs, the JK trigger has a C control (actuation) control input, as well as an input terminal R and S. Constituent inputs have priority over all others. The active signal level at the input S sets the JK trigger to the state $Q = 1$, and the active level of the signal at the input R - to the state $Q = 0$, regardless of signals from other inputs. If the input voltages are at the same time applied to the passive signal level, the trigger state will change at pulse recession at the input input, depending on the input state J and K.

A counter is a digital memory node built on triggers, which can be in one of the 2^n states, where n is the number of triggers. The digit count n is

equal to the number of T triggers. Each input pulse changes the state of the counter, which persists until the next signal is received. The counter is one of the main functional nodes of the computer, as well as various digital controllers and information-measuring systems.

Characteristics:

- a) information capacity is determined by the number of states in which the meter may be;
- b) speed - maximum frequency of passage of pulses on the counter input.

Registers are triggers and data storage nodes.

Motion of work

Experiment 1 - research RS - trigger

- 1 Draw a diagram depicted in Fig. 2.1 (file 14_02 in the examples)
- 2 When changing the state at the inputs S, R, use the "S" and "R" switches to fill in the table 2.1

Experiment 2 - study JK - trigger

- 1 Make the JK scheme - a flip-flop, depicted in Fig. 2.2 (file 14_03 in the examples)
- 2 Fill in the table 2.2. Set the JK trigger to its original state by specifying the sequence of incoming sets according to Table 2.2.
- 3 Fill in table 2.3 by specifying the sequence of input kits using the "J", "K", "C"

Experiment 3 - study of the counter

- 1 Draw the schema shown in Figure 2.3 (file 14_06 in the examples)
- 2 Use the C switch to change the status of the counters. Enter the current states in Table 2.4

1 k Ohm /5 V

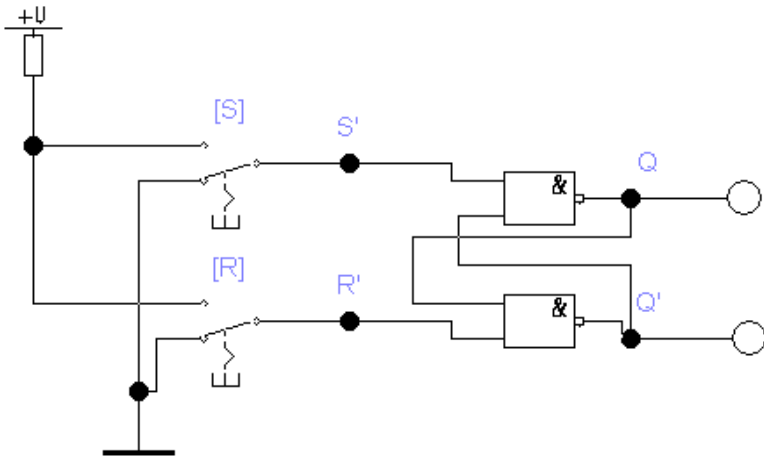


Figure 2.1 - Study scheme of RS-trigger

Table 2.1 - Transaction table

R	S	Q	Q'	Mode
0	1			
1	1			
1	0			
1	1			
0	0			

Table 2.2 - Asynchronous table of JK-flip-flop transitions

S	R	Q	Q'
0	1		
0	0		

Experiment 4 - study of a counter with a variable conversion factor

1 Draw the schema shown in Figure 2.4 (file 14_08.ca4 in the examples)

2 Fill in the table 2.5

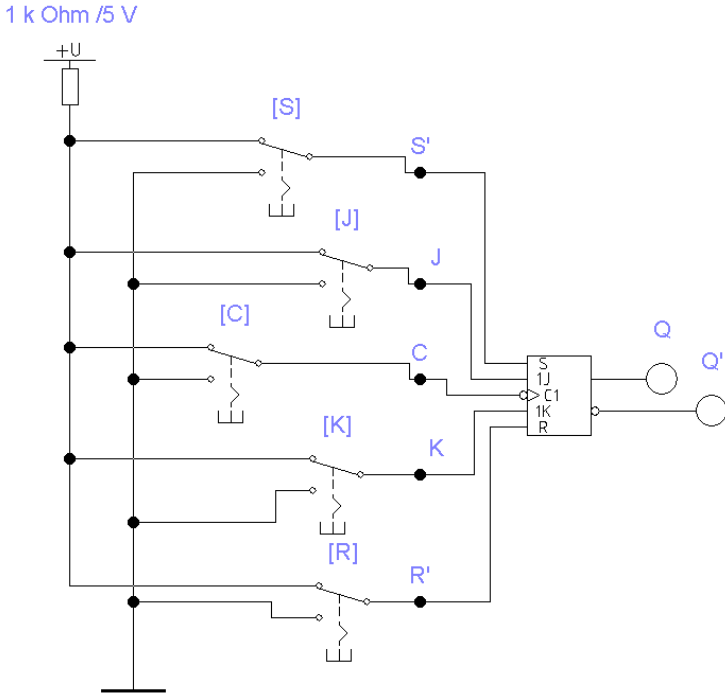


Figure 2.2 - Study scheme of the JK-trigger

Table 2.3 - Input kits, states and operating modes of the JK-trigger

S	R	J	K	C	Q	Mode
0	0	0	0	0		
0	0	0	0	1		
0	0	0	0	0		
0	0	1	0	0		
0	0	1	0	1		
0	0	1	0	0		
0	0	0	1	0		
0	0	0	1	1		
0	0	0	1	0		
0	0	1	1	0		
0	0	1	1	1		
0	0	1	0	1		

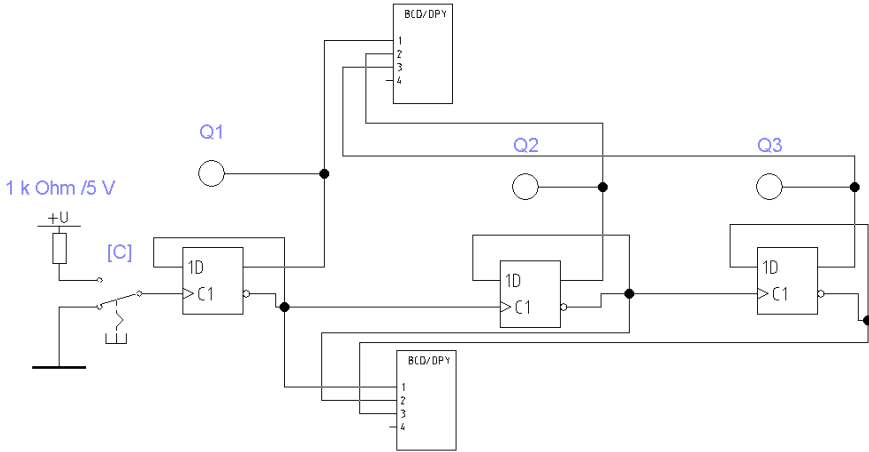


Figure 2.3 - Scheme of research of three-bit binary counter

Experiment 5 - synthesis of a counter with a given coefficient of recalculation type (aggravated, subtracting)

1 Upgrade the circuit (Figure 2.4) in accordance with the individual task of the meter parameters

2 Check experimentally the table of states of the counter

Таблиця 2.4 – Таблиця станів лічильника

The state of the upper BCD / DPY	The state of the lower BCD / DPY	The state of the triggers Q3 Q2 Q1

Table 2.5 - Table of states of the counter

Input pulse number	State counter by indicator	The state of the triggers Q3 Q2 Q1
0		
1		
2		
3		
4		
5		

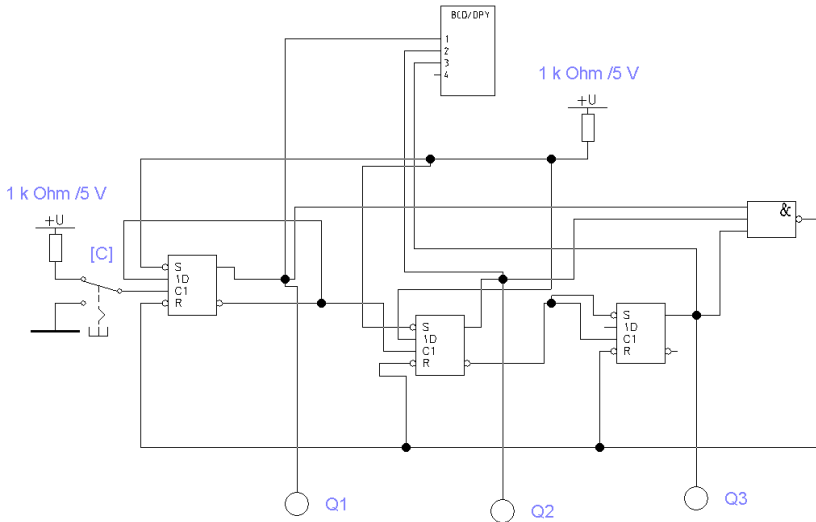


Figure 2.4 - A counter with a variable conversion factor

Control questions

1. Determination of nodes with memory
2. Typical memory nodes
3. Classification of flip-flops, characteristics of counters, principles of operation of flip-flops, counters, registers.
4. Construction of a counter with a given conversion factor

LABORATORY WORK 3

Objective: to study the structure and principle of the compensating voltage regulator. Investigate the voltage limits of the stabilizer and its load characteristics. Brief theoretical data: a voltage regulator is a device that automatically maintains a constant voltage on the load. It is characterized by the following parameters:

- the coefficient of stabilization - the relation of the instability of the input voltage to the instability at its output:

$$K_c = \frac{\frac{\Delta U_{\text{ex}}}{U_{\text{ex.НОМ}}}}{\frac{\Delta U_{\text{eux}}}{U_{\text{eux.НОМ}}}}$$

where ΔU_{ex} , ΔU_{eux} - change the input and output voltages respectively, $U_{\text{ex.НОМ}}$, $U_{\text{eux.НОМ}}$ - nominal input and output voltages respectively;

- internal (output) resistance - this is the ratio of change in the output voltage ΔU_{eux} to the change in load current ΔI_{eux} , which caused the change in voltage:

$$r_i = \frac{\Delta U_{\text{eux}}}{\Delta I_{\text{eux}}}$$

- - temperature coefficient voltage (TCV) - the ratio of voltage ΔU_{eux} change to the change in ambient temperature Δt that caused the change in voltage:

$$TCV = \gamma = \frac{\Delta U_{\text{eux}}}{\Delta t}$$

In principle, the stabilizers are divided into compensatory and parametric ones. The principle of operation of parametric stabilizers is based on the use of devices that have non-linear volt-ampere characteristics. Silicon stabilizers are used to build such stabilizers. Compensation stabilizers work as a closed-loop automatic feedback control system.

Motion of work

Experiment 1 - Research of the minimum allowable input voltage.

1 Collect the diagram shown in Fig. 3.1 (Regulate in the Samples folder)

2 Increase voltage source V7 (see Figure 3.1)

3 Observe the input and output voltage form on the oscilloscope

3 Repeat items 2, 3 until the distortion of the output voltage form appears. Record the limit value of the input voltage.

Experiment 2 - Research of the maximum allowable input voltage

1 Update the initial value of $V7 = 0.707V$

2 Increase the voltage of the $V8$ source (see Fig. 3.1).

3 Observe the input and output voltage form on the oscilloscope

4 Repeat items 2, 3 until the shape of the output voltage is distorted.

Record the limit value of the input voltage.

Experiment number 3 - Study of the load characteristics of the stabilizer

1 Update the initial values of $V7$, $V8$.

2 Change the $R25$ and fix the U_{out} . Results are listed in Table 3.1.

3 Repeat item2 until the U_{out} decreases by 10% from the $U_{out\ nom} = 13.5\ V$.

4 Fix the resistance at which $U_{out} = 13.5\ V$ as the maximum permissible resistance.

Table 3.1 – Results of measurements

$U_{out},\ B$							
$R_{25},\ \Omega M$							
$I_{out},\ A$							

5. Build a graph of the dependence of U_{out} and I_{out} , and determine the limits of permissible resistance.

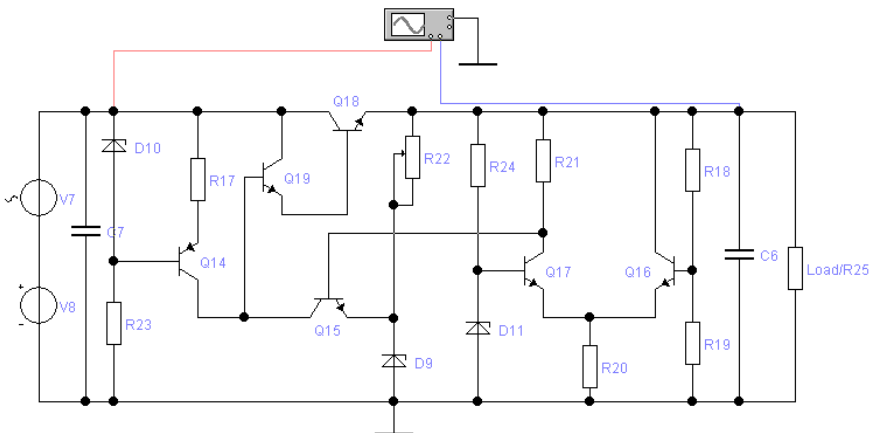


Figure 3.1 - Principle diagram of the compensating stabilizer

Legend:

Q17, Q16, R21, R20 - comparison scheme;

D11, R24 - reference voltage source;

V7, V8 - creates an input chain model;

Q18, Q19 - an element regulated on a composite transistor;

Q14, R17, R23, D10 - current sources;

R18, R19 - voltage dividers;

R22, Q15, D9 - amplifier;

R25 - load.

Control questions

1. The principle of the parametric stabilizer.
2. Principle of action of compensating stabilizer.
3. Block diagram of parametric and compensating stabilizers.
4. Concept of a serial and parallel compensating stabilizer.
5. Assignment of elements of the scheme under study.

LABORATORY WORK 4

Objective: to study the structure and operation of the DAC and ADC.

Brief theoretical data: the main task of the ADC is the development of binary signal codes - a periodic sampling of the analog signal. According to the principle of operation, all existing ADC types can be divided into 2 groups:

- ADC with charge capacitor;

- ADC with comparison of the input signal with discrete voltage levels.

The principle of the operation of the DAC is to convert the digital code to resistance or load, which is why the main devices of the DAC are decoder input code with control keys and the resistor circuit. A simple DAC can be built on the basis of an inverting adder.

Motion of work

Experiment number 1 - DAC research on the basis of an inverting adder

1 Collect the diagram shown in Fig.4.1

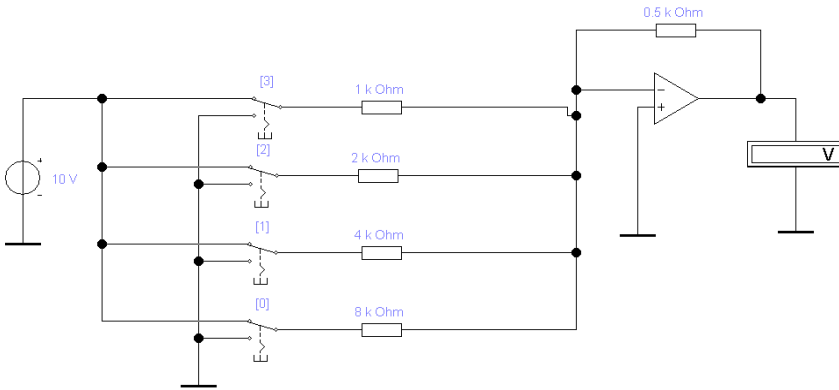


Figure 4.1 - DAC based on an inverting adder

2. Use the 0-3 switches to set different binary codes at the DAC input and observe the output voltage of the DAC. Include the results in Table 4.1.

Table 4.1 - DAC research based on an inverting adder

3	2	1	0	U_{out}

3 Determine the number of graduations, the output voltage range, and the maximum conversion error

Experiment 2 - Research of DAC with resistive matrix R-2R

1. Collect the diagram shown in Fig. 4.2.

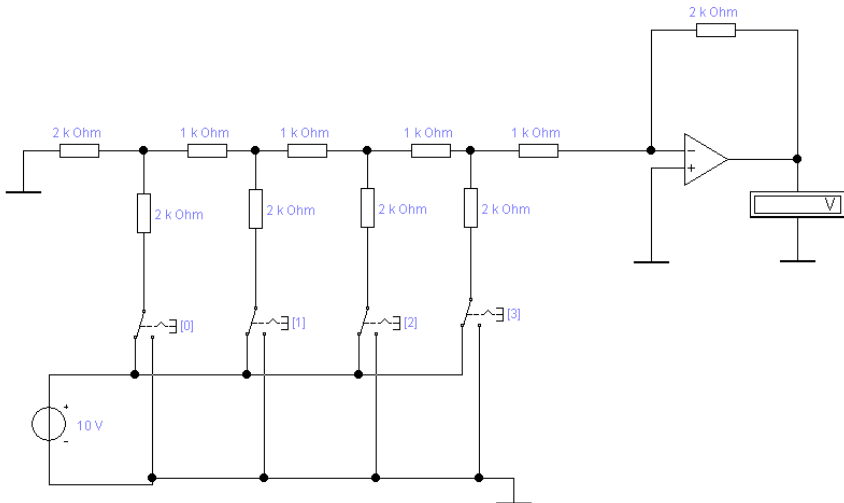


Figure 4.2 - DAC with resistive matrix R-2R

2. Use the "0-3" switches to set different binary codes at the DAC input and observe the output voltage of the DAC. Include the results in Table 4.2.

3. Determine the number of graduations, the range of the output voltage and the maximum error of the transformation.

Table 4.2 - Research DAC with resistive matrix R-2R

3	2	1	0	U_{out}

Experiment 3 - DAC research based on the EWB library

1 Collect the schema shown in Figure 4.3

2 The word generator is programmed into the cyclic mode of word sequence execution (0000, 0001, ... 00FE, 00FF) with a frequency of 1 kHz

3 Using the oscilloscope to observe the voltage dependence on the output of the DAC from time to time. The oscillogram is redrawn to the report.

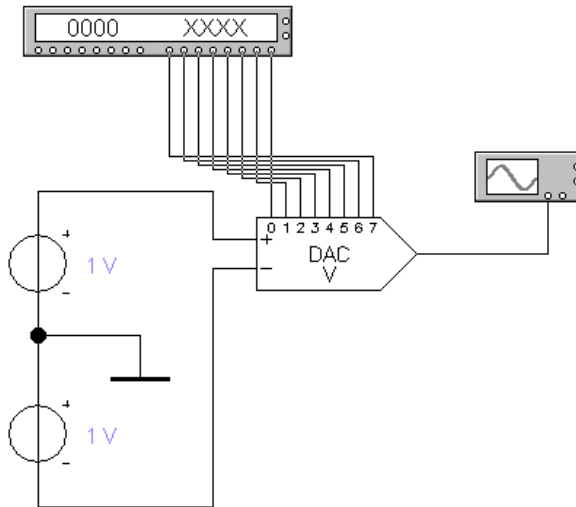


Figure 4.3 - DAC based on the EWB library

Control questions

1. Advantages and Disadvantages of DAC Based on Inverting Adder and Resistive Matrix R-2R
2. Purpose and structure of ADC
3. Principle of DAC operation
4. What determines the error of the DAC, the range of output voltage, the number of graduations of the output voltage

LABORATORY WORK 5

Objective: to study the structure and principle of the unipolar power regulator.

Brief theoretical data: The power regulator is designed to control the average power in the load. It consists of a power transformer, a power element and a control circuit. Power elements are performed on thyristors, thyristors or opto-thyristors. The control circuit is based on digital or analog principles and controls the delay of activating power elements

relative to the moment of the transition time through the zero voltage of the network.

In this paper, a digital control circuit is investigated, in which the control signal code is entered in the subtractive counter at the moment of the network voltage transition through zero. Under the action of clock pulses state of the meter decreases. The signal for the activation of the power elements is formed at the moment of the switch of the counter to "0".

Motion of work

Experiment 1 – Research of the synchronization node with the power supply

1 Collect the diagram shown in Fig. 5.1

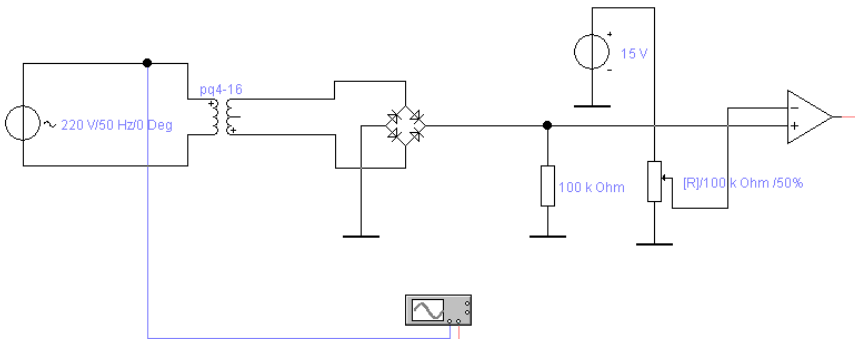


Figure 5.1 - Reseach of network synchronization node

1 Watch at the output of the node short pulses of synchronization at the moment of zero voltage transition. Using the potentiometer and changing the conversion factor of the pq 4-16 transformer, maximally reduce the width of the pulses of synchronization. Determine the width of the pulses.

2 The oscillograms of the voltage at the output of the transformer and the output of the synchronization node are redrawn into the report.

Experiment 2 - Research of the control circuit of the digital power regulator

1. Add the previous diagram (Fig. 5.1) to the elements of the controlled digital delay as shown in Fig. 5.2.

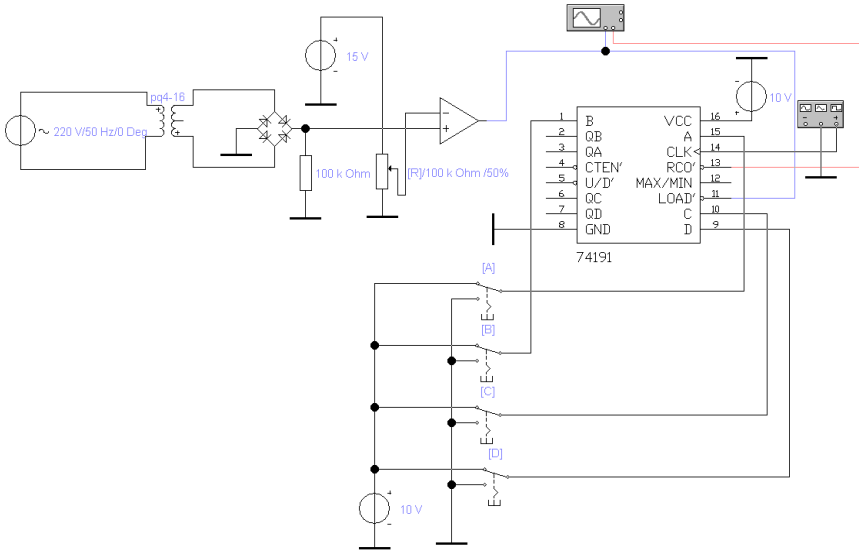


Figure 5.2 - Digital control circuitry of the power regulator

2. To adjust the generator to the mode of formation of rectangular pulses with frequency:

$$f = 2f_c(2^m - 1)$$

where f_c is the frequency of the network voltage; m - the number of digits in the code ($m = 4$).

3 Set the various control codes using the "A", "B", "C", "D" switches. Measure the time delay of the pulse on activating the power element (RCO output) relative to the pulse of synchronization (LOAD input). Put results in the table, build a dependency graph $T_{\text{delay}} = f(\text{code})$.

Control questions

1. Structural scheme of the control unit.
2. One is a bipolar controller.
3. Principles of network synchronization node operation.
4. Types of power elements.

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